**ÇANKAYA UNIVERSITY – ECE DEPARTMENT – ECE 376**

**2015 Spring Term May 2015**

**Experiment 13: Creating and running the hardware cosimulation (hwcosim) of 8 PSK modulator and demodulator on Xilinx Virtex-5 FPGA card**.

**Experiment constructed from Matlab Simulink Xilinx blocks is given on course webpage with the names “PSK\_Exp13\_HWcosim.mdl” and “CorrMHTE.m”**

1. Download the model file and the m file from the course web page and start Matlab from Xilinx Design Tools → ISE Design Suite 14.2 → System Generator → System Generator. Open the model file, **“PSK\_Exp13\_HWcosim.mdl”.** It should look like the configuration given in Fig. 1. Note that **PSK\_Exp13\_HWcosim.mdl** is the same as **PSK\_Exp12\_Pe.mdl** in Experiment 12, with transmitter, noise and receiver blocks converted to one single subsystem.
2. Following the steps in the notes of “**Virtex-5 HWCo\_HTE\_23032015”**, create on your computer the hardware cosimulation facility.
3. Press “System Generator” token in **PSK\_Exp13\_HWcosim.mdl**. From there, select Compilation → Hardware Co-Simulation → Virtex5. Make sure that Virtex-5 FPGA card is electrically swicted on. Finally by pressing “Generate” button, the operation will start and end (after 10-20 minutes) by creating the hwcosim block in a blank model file. Copy and paste this block into **PSK\_Exp13\_HWcosim.mdl**. Your new model file should look like the one shown in Fig. 2.
4. Connect to the output of **PSK\_Exp13\_HWcosim hwcosim** block to theError Rate Calculation block and the Scope. then run the whole model file and observe that the displays for both the simulink setup and the hwcosim setup deliver the same or similar probability of error values. For reference purposes, the theoretical probability of error graphs of Proakis 2002 is pasted in Fig. 3. Bear in mind that the residual error previously encountered in the “Display” is not applicable in this experiment.

Fig.1 The model file “**PSK\_Exp13\_HWcosim.mdl**”.



Fig.3 Probability of error curves in Fig. 7.57 of Proakis 2002.